- 6. What are different types of operators in VHDL? Write the operator precedence table. Write a VHDL program to illustrate the logical shift operation. 3+3+4=10
- 7. Design a 4:1 MUX using 2:1 MUXs. Write the corresponding VHDL program. 5+5=10
- 8. Write short notes on any two. $5 \times 2=10$
 - (i) Floating point numbers.
 - (ii) Arithmetic logic unit.
 - (iii) Control logic.

2023/ODD/12/33/MECE-301/025

M. Tech Odd Semester Examination, February, 2023

Electronics & Communication Engineering (3rd Semester)

Course No.: MECE-301A (Hardware Description Language)

Full Marks: 50 Pass Marks: 25

Time: 2 hours

- Note: 1. Attempt any five questions.
 - 2. Begin each answer in a new page.
 - 3. Answer parts of a question at a place.
 - 4. Assume reasonable data wherever required.
 - 5. The figures in the right margin indicate full marks for the question.
 - 6. All the mathematical symbols and abbreviations have their usual meanings.
- 1. Design a 4-bit adder/subtractor and write the corresponding VHDL program using structural modelling style. 4+6=10
- 2. How different types of delay are modelled in VHDL? Explain each of them with suitable example of VHDL codes. 5+5=10
- 3. What are the different modelling styles in VHDL? Write a VHDL program to illustrate the mixed modelling style. 2+8=10
- 4. What do you mean by state machines? Write VHDL programs for Moore and Melay machines.

(3+3)+4=10

5. Write a VHDL program using process statement to design a negative edge triggered D-type flip-flop with direct preset and reset inputs. Using the same design a 4-bit shift register. 6+4=10