M. Tech Odd Semester Examination, February, 2023

Electronics & Communication Engineering

(1st Semester)

Course No.: MECE-102

(Digital VLSI Design)

Full Marks: 70
Pass Marks: 28

Time: 3 hours

Note:
1. Attempt 05 (Five) questions by taking one form each unit.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the right margin indicate full marks for the question.

UNIT-I

1. a) Draw the energy-band diagram of MOS system under different gate bias conditions and explain the principle of operation.

   b) Discuss the short-channel effects in details. 6+8=14

2. a) Derive the expression for threshold voltage in a MOSFET considering substrate bias.

   b) What do you mean by design rules?

   c) Draw the layout of a CMOS inverter and explain the layers used. 6+4+4=14

UNIT-II

3. a) Design the following logical expression using static CMOS and pseudo nMOS logic and explain their working principle.

b) What is TG logic? Design an XOR logic using TG logic and explain its working principle. 8+6=14

4. a) Derive the expression for rise and fall time of a CMOS inverter.

b) Derive the expression for noise margins of a CMOS inverter. 6+8=14

UNIT-III

5. a) Draw the circuit diagram of a JK latch using static CMOS logic and explain its working principle.

b) Draw the circuit diagram of a positive edge triggered D flip-flop using TGs and inverters and explain its working principle. 6+8=14

6. a) What is dynamic CMOS logic?

b) What are issues of a dynamic CMOS logic?

c) How the issues are resolved using domino logic – explain with a suitable example. 4+4+6=14

UNIT-IV

7. a) What is BiCMOS logic?

b) What are the advantages of BiCMOS logic over CMOS logic?

c) Design a NAND gate using BiCMOS logic and explain its working principle. 4+4+6=14

8. a) Draw the circuit diagram of SRAM circuit and explain the read and write operations.

b) Draw the circuit of dynamic RAM circuit and explain its operation.

c) Compare SRAM vs. DRAM circuit. 6+6+2=14

UNIT-V

9. a) What is HDL? Discuss different HDL for design of digital logic circuits.

b) Draw the front-end VLSI design flow and explain its components.

c) Draw a mealy machine and explain. 6+4+4=10

10. a) What are the different design styles available in VHDL? Explain.

b) Draw the architecture of FPGA and explain its components.

c) What is ESD protection circuit? 6+4+4=10

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