5. Discuss the MOSFET scaling techniques with their merits and demerits. 10

6. Design a master-slave D flip-flop using a combination of the static CMOS and transmission gate logic and explain its working principle. 6+4=10

7. Design a combinational logic circuit using static CMOS and pseudo-nMOS logic to implement the following function. Explain their working principle. 3+3+2+2=10

$$Y = \overline{AB + CDE}$$

8. What is dynamic CMOS logic? What is the problem of this logic and how this can be solved using domino CMOS logic. 3+2+5=1

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B. Tech Odd Semester Examination, February, 2023

Electronics & Communication Engineering

(5th Semester)

Course No.: EC-CC-14

(Digital VLSI Design)

Full Marks: 50

Pass Marks: 15

Time: 2 hours

Note:
1. Attempt any five questions.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the right margin indicate full marks for the question.
6. All the mathematical symbols and abbreviations have their usual meanings.

1. Draw the VTC of a CMOS inverter and derive the expression for the critical voltages: V_{IL}, V_{IH}, V_{OL}, and V_{OH}. 2+2+2+2+2=10

2. What is latch up in CMOS circuits? Explain with necessary diagram and discuss its remedial techniques. 2+6+2=10

3. What is pass transistor and transmission gate logic? Draw the small signal equivalent circuit model of an nMOS transistor and derive the expressions for transconductance and output resistance.

2+2+2+2+2=10

4. What are different types of design rules? Draw the stick diagram of a NOR gate and its layout. Derive the expression for propagation delay of a CMOS inverter. 2+2+2+4=10