B.Tech Odd Semester (CBCS) Exam., December—2016

INFORMATION TECHNOLOGY

(3rd Semester)

Course No. : IT-305

(Digital Electronics)

Full Marks : 75
Pass Marks : 30

Time : 3 hours

Note : 1. Attempt one question from each Unit.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the right margin indicate full marks for the question.

UNIT—1

1. *(a)* What are the three stages for designing of digital systems? Explain each of them. 1+2+2+2=7

(b) Convert the following binary numbers to gray code numbers : 2×4=8

(i) 00111

(ii) 1111

(iii) 1101

(iv) 1001

2. *(a)* Encode data bits 0011 into the 7-bit even parity Hamming code. 5

(b) Write all the methods of obtaining the 2's complement of a number. 5

(c) Subtract the following in BCD and XS-3 codes : 5

(i) 920–265

(ii) 635·7–419·8

UNIT—2

3. *(a)* Simplify the following Boolean functions and draw the logic diagram : 5+5=10

(i) $F(A, B, C, D)$ (1, 2, 4, 6, 7)

(ii) $F(A, B, C, D)$ (4, 5, 6, 7, 8, 12)
d(1, 2, 3, 9, 11, 14)

(b) Express the Boolean function $F = xy + xz$ in a product of maxterm form using the distributive law. 5

4. *(a)* Simplify the following Boolean expression to a minimum number of literals : 5

$$xyz \quad x\,y \quad xyz$$

(b) Expand $A \quad B$ to minterms and maxterms. 5

(c) Reduce the expression

$$(a \quad b)\,(a \quad \overline{b})\,(\overline{a} \quad \overline{b})$$

in POS form using K-map. 5

UNIT—3

5. *(a)* Design a combinational circuit to produce an output of 1, when its input is a 2421 code representing an even decimal number less than 10, otherwise 0. 5

(b) Show two 3-to-8 line decoders with enabled and inputs connected to form a 4-to-16 line decoder. 5

(c) Implement a full-adder with two half-adders and an OR gate. 5

6. *(a)* Design a 3-to-8 line decoder using two 2-to-4 line decoders. 5

(b) Construct a 32×1 MUX using 8×1 MUX and 4×1 MUX. 5

(c) Design a Borrow look-ahead subtractor. 5

UNIT—4

7. *(a)* Design a 4-bit synchronous binary counter using D flip-flop. 8

(b) Convert SR flip-flop to D flip-flop and design the logic diagram. 5

(c) What do you mean by Race-Around condition? 2

8. *(a)* A sequential circuit has two JK flip-flops A and B and one x. The circuit is described by the following flip-flop input equations :

$$J_A \quad x \qquad K_A \quad B$$
$$J_B \quad x \qquad K_B \quad A$$

(i) Derive the state equation $A_{(t\ 1)}$ and $B_{(t\ 1)}$ by substituting the input equations for J and K variables.

(ii) Draw the state diagram of the circuit. 8

(b) Explain, in detail, the working of Johnson counter. What are the differences between Ring counter and Johnson counter? 4+3=7

UNIT—5

9. *(a)* Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and outputs a binary number equal to the square of the input number. 8

(b) What are the different types of series comes in TTL gates? 3

(c) Describe the basic circuit of open-collector TTL NAND gates. 4

10. *(a)* Design a 32×8 ROM. 8

(b) What are the basic types of MOS structure? 3

(c) Discuss the symbols for MOS transistor. 4

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