B.Tech Odd Semester (CBCS) Exam., December—2016

COMPUTER SCIENCE AND ENGINEERING

(3rd Semester)

Course No. : CSECC-03

(Digital Electronics)

Full Marks : 50
Pass Marks : 15

Time : 2 hours

Note : 1. Attempt *any* **five** questions.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the margin indicate full marks for the questions.

1. *(a)* What is special case in 2's complement form? Express –73·75 in 12-bit 2's complement form. 1+4=5

(b) Show that (A B)(AB) is equivalent to A B or not. 5

2. *(a)* Implement combinational circuit that converts a 3-bit gray code to a binary number only using Ex-OR gates. 5

(b) Simplify the following Boolean function into SOP and POS forms using K-map : 5

$F(A, B, C, D)$ (3, 4, 6, 7, 11, 12, 13, 14, 15)

3. *(a)* Simplify the logic function

$f(A, B, C, D, E)$
(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)

using the Quine-McCluskey method. 5

(b) Design a carry look-ahead adder (CLA). 5

4. *(a)* Design a minimal circuit to produce an output of 1, when its input is a 2421 code representating an even decimal number less than 0. 5

(b) Implement a 4 16 decoder with the help of 2 4 decoder having enable inputs. 5

5. *(a)* Convert SR flip-flop to JK flip-flop and draw the logic diagram. 4

(b) Using the following input equation, derive the circuit, state table and state diagram : 6

J_A B, K_A x B, J_B x
K_B A x

6. *(a)* Draw the logic diagram of 4-bit ring counter using D flip-flop. 3

(b) Design and implement of a synchronous 3-bit up/down counter using JK flip-flop. 7

7. *(a)* Design a mod-8 up asynchronous counter using JK flip-flop. 4

(b) Reduce the number of states in the following state table, and tabulate the reduce state table and draw the state diagram : 6

Present state	*Next state*		*Output*	
	x 0	x 1	x 0	x 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

8. *(a)* Explain in detail the working principle of master-slave flip-flops with the help of logic diagram and timing diagram. 6

(b) Design a 32 8 ROM. Each unit consists of 32 words of 8-bit each. 4

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