B.Tech Odd Semester (CBCS) Exam., December—2016

INFORMATION TECHNOLOGY

(7th Semester)

Course No. : IT–705B

(VLSI Design and Testing)

Full Marks : 75
Pass Marks : 30

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **five** questions, taking **one** from each Unit

UNIT—I

1. *(a)* Define the following terms :

IC, Die, VLSI, Feed through cell, Aspect ratio

(b) Briefly discuss all the steps of the VLSI design cycle. What are the major contributing factors of new trends in the industry of VLSI design? 5+(8+2)=15

2. *(a)* Describe three major steps of VLSI physical design cycle. How can we reduce interconnect delay in physical design?

(b) Compare different design styles with respect to cell size, cell placement, interconnection and design cost. Why full custom design style is usually used for microprocessor? (6+2)+7=15

UNIT—II

3. *(a)* What is a High Level Synthesis (HLS) for VLSI design? Describe various steps of HLS with help of a diagram.

(b) Differentiate between the time constrained and resource constrained schedulings. Find out a solution of resource constrained scheduling for $(a \quad b \quad c \quad d)^* \, e$, where one adder and one multiplier are available. (2+6)+(4+3)=15

4. *(a)* What is allocation and binding in HLS? Differentiate between storage binding and functional unit binding.

(b) Define clique partitioning. Formulate the functional unit allocation as a clique partitioning problem. Explain Tseng's algorithm with help of an example. (2+3)+(2+3+5)=15

UNIT—III

5. *(a)* How can we formulate the partitioning problem? Explain the constraints and objective function for the partitioning algorithms.

(b) Explain all the steps of Kernighan-Lin (KL) algorithm with example. Mention two disadvantages of KL algorithm. (2+5)+(6+2)=15

6. *(a)* What are slicing floor plan and non-slicing floor plan? Explain rectangular dualization based floor planning using an example. What are the drawbacks of this method?

(b) Define channel routing and switch-box routing. Differentiate horizontal constraint graph (HCG) and vertical constraint graph (VCG) for a channel routing problem. (3+3+1)+(3+5)=15

UNIT—IV

7. *(a)* Differentiate between verification and testing in context of VLSI. What are various types of test for testing a chip? Explain the digital VLSI test process with a diagram.

(b) Describe test economics for a VLSI testing process. (3+3+4)+5=15

8. *(a)* Give a comparative analysis of functional testing and structural testing.

(b) Find the test patterns to detect all stuck-at-fault for an AND gate. Justify your answer. Explain fault equivalence and fault collapsing with examples. 5+(4+6)=15

UNIT—V

9. *(a)* What is test pattern? What is the source of test pattern? Explain steps that are involved to generate a test pattern.

(b) What are the basic principles of fault simulation? Describe serial fault simulation with examples. (1+2+5)+(2+5)=15

10. Write short notes on the following : 7½+7½=15

(a) Parallel fault simulation

(b) Built-in self-test (BIST)

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